SEMICONDUCTOR DEVICE WITH RECOMBINATION REGION

BACKGROUND

Semiconductor devices like semiconductor diodes, IGFETs (insulated gate field effect transistors) and IGBTs (insulated gate bipolar transistors) include a pn junction. When the pn±junction is forward biased, mobile charge carriers flood the semiconductor regions on both sides of the pn junction. Where at least one of these regions is formed as a drift zone with comparatively low impurity concentration and comparatively large extension along a current flow direction, the charge carriers may form a charge carrier plasma that has to be removed from the drift layer when the pn junction switches from forward biased to reverse biased. Removing the charge carrier plasma from the drift zone is known as reverse recovery and contributes to the dynamic switching losses of the semiconductor device. It is desirable to provide semiconductor devices with improved switching characteristics.

SUMMARY

An embodiment refers to a semiconductor device including a drift zone in a semiconductor body. A charge-carrier transfer region forms a pn junction with the drift zone in the semiconductor body. A control structure electrically connects a recombination region to the drift zone during a desaturation cycle and disconnects the recombination region from the drift zone outside the desaturation cycle.

Another embodiment is related to a controllable semiconductor diode including a drift zone in a semiconductor body. A charge-carrier transfer region forms a pn junction with the drift zone in the semiconductor body. A control structure electrically connects a recombination region to the drift zone during a desaturation cycle and disconnects the recombination region from the drift zone outside the desaturation cycle.

A further embodiment concerns an insulated gate bipolar transistor including a drift zone in a semiconductor body. A charge-carrier transfer region forms a pn junction with the drift zone in the semiconductor body. A control structure electrically connects a recombination region to the drift zone during a desaturation cycle and disconnects the recombination region from the drift zone outside the desaturation cycle.

Those skilled in the art will recognize additional features and advantages upon reading the following detailed description and on viewing the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification. The drawings illustrate the embodiments of the present invention and together with the description serve to explain principles of the invention. Other embodiments of the invention and intended advantages will be readily appreciated as they become better understood by reference to the following detailed description.

FIG. **1**A is a schematic cross-sectional view of a portion of a semiconductor device with a body pn junction for illustrating aspects of the embodiments.

FIG. **1**B is a schematic cross-sectional view of a portion of a semiconductor device according to an embodiment related to a vertical pn junction.

FIG. **1**C is a schematic cross-sectional view of a portion of a semiconductor device according to an embodiment related to a horizontal pn junction.

FIG. **2**A is a schematic cross-sectional view of a portion of a semiconductor device in accordance with an embodiment related to a semiconductor diode.

FIG. **2**B is a schematic cross-sectional view of a portion of a semiconductor device in accordance with an embodiment related to an IGFET.

FIG. **2**C is a schematic cross-sectional view of a portion of a semiconductor device in accordance with an embodiment related to an IGBT.

FIG. **2**D is a schematic cross-sectional view of a portion of a semiconductor device in accordance with an embodiment related to an RC-IGBT (reverse conducting IGBT).

FIG. **3**A is a schematic plan view of a semiconductor body of a semiconductor diode according to an embodiment providing evenly distributed compact desaturation cells.

FIG. **3**B is a schematic plan view of a semiconductor body of a semiconductor diode according to an embodiment providing stripe-shaped desaturation cells.

FIG. **3**C is a schematic plan view of a semiconductor body of a semiconductor diode according to an embodiment providing a grid-like desaturation cells.

FIG. **3**D is a schematic plan view of a semiconductor body of a semiconductor diode according to an embodiment providing unevenly distributed compact desaturation cells.

FIG. **4**A is a schematic plan view of a semiconductor body of a semiconductor device including evenly distributed compact desaturation and transistor cells.

FIG. **4**B is a schematic plan view of a semiconductor body of a semiconductor device including regularly arranged transistor and desaturation cells.

FIG. **4**C is a schematic plan view of a semiconductor body of a semiconductor device including a grid-shaped desaturation cell and transistor cells formed in the meshes of the desaturation cell.

FIG. **4**D is a schematic plan view of a semiconductor body of a semiconductor device including a frame-like desaturation cell and evenly distributed compact transistor cells.

FIG. **5**A is a schematic cross-sectional view of a portion of a semiconductor device according to an embodiment providing recombination regions in a bottom region of a cavity.

FIG. **5**B is a schematic diagram showing the diode characteristics of the semiconductor device of FIG. **5**A.

FIG. **5**C is a schematic diagram showing current flow lines and electron density in the semiconductor device of FIG. **5**A at the disabled recombination region.

FIG. **5**D is a schematic diagram showing current flow lines and the electron density in the semiconductor device of FIG. **5**A at enabled recombination region.

FIG. **5**E is a schematic diagram illustrating a plasma charge at different states of the semiconductor device of FIG. **5**A.

FIG. **6**A is a schematic circuit diagram of a semiconductor device according to an embodiment including an IGBT and a control circuit for generating an internal desaturation signal for the IGBT.

FIG. **6**B is a schematic time chart showing a step signal response of the control circuit of FIG. **6**A.

FIG. **6**C is a schematic time chart illustrating a square signal response of the control circuit of FIG. **6**A.